LISTING OF CLAIMS

1-10. (Canceled)

11. (Currently Amended) A semiconductor wafer comprising:

at least one active area;

at least one discrete resistor having a resistive region obtained within said active area, the discrete resistor having first and second ends to which metal contacts are formed; ~~and~~

a delimitation structure set on top of said active area as an ion implantation mask to delimit a size and shape of ion implantation which forms said resistive region, the delimitation structure defining a width of the discrete resistor between the first and second ends; and

a silicide layer formed over the delimitation structure which does not electrically contact the resistor region.

12. (Original) The wafer according to claim 11, wherein said delimitation structure is made of a material used in the semiconductor industry.

13. (Original) The wafer according to claim 12, wherein said delimitation structure is made of a material selected from a group consisting of a dielectric, a semiconductor and a metal.

14. (Original) The wafer according to claim 12, wherein said delimitation structure is made of polysilicon.

15. (Previously Presented) The wafer according to claim 11, further comprising a protective element which extends within said delimitation structure and coats said resistive region.

16. (Previously Presented) The wafer according to claim 15, wherein said protective element is made of a dielectric material.

17. (Previously Presented) An integrated device comprising:

a semiconductor substrate;

at least one active area on the semiconductor substrate;

at least one resistor region within said active area, the resistor region having first and second ends to which metal contacts are formed;

a delimitation structure set on top of said active area as an ion implantation mask to delimit a size and shape of ion implantation which forms said resistor region in the semiconductor substrate, the delimitation structure defining a width of the resistor region between the first and second ends; and

a silicide layer formed over the delimitation structure which does not electrically contact the resistor region.

18. (Original) The integrated device according to claim 17, wherein said delimitation structure is made of a material used in the semiconductor industry.

19. (Original) The integrated device according to claim 18, wherein said delimitation structure is made of a material selected from a group consisting of a dielectric, a semiconductor and a metal.

20. (Original) The integrated device according to claim 18, wherein said delimitation structure is made of polysilicon.

21. (Previously Presented) The integrated device according claim 17, further comprising a protective element which extends within said delimitation structure and coats said resistor region.

22. (Previously Presented) The integrated device according to claim 21, wherein said protective element is made of a dielectric material.

23-31. (Canceled)

32. (Currently Amended) An integrated circuit, comprising:

a substrate including an active region;

a discrete resistor formed within the active region of the substrate, the discrete resistor having first and second ends to which metal contacts are formed;

a delimiter structure formed over the substrate and defining a mask used for ion implantation, but not comprising a transistor gate structure of the integrated circuit, to form and define a size and shape of the discrete resistor;

a spacer extending between the delimiter structure to cover the discrete resistor formed in the active region but not cover a top surface of the delimiter structure; and

a silicided layer formed on the delimiter structure without being in electrical contact with the metal contacts of the resistor.

33. (Currently Amended) An integrated resistive element having protection from silicidation, comprising:

at least one active area in a semiconductor substrate;

at least one resistive region having a pre-set resistivity in said active area;

a silicided delimitation structure on top of said active area that delimits a width of said resistive region but is not in electrical contact with the resistive region;

a pair of electrical metal contacts positioned at opposite ends of a length of the resistive region; and

a protective structure which protects said resistive region from salicidation, extends within said delimitation structure and covers said resistive region.

34. (Previously Presented) The element according to claim 33, wherein said protective structure is made of a material selected from the group consisting of: silicon dioxide, silicon nitride, and silicon oxynitride.

35. (Previously Presented) The element according to claim 33, wherein said delimitation structure is made of polysilicon.

36. (Previously Presented) An integrated circuit, comprising:

an active area defined in a semiconductor substrate;

a resistive region having a pre-set resistivity formed in the active area;

a polysilicon structure, which is not a transistor gate structure of the integrated circuit, defining a mask which delimits a width of ion implantation which forms the resistive region;

a protective layer over the resistive region between the polysilicon structure; and

a silicided layer formed on the polysilicon structure without affecting the pre-set resistivity in the active area and which does not electrically make contact with the resistive region.

37. (Previously Presented) The circuit according to claim 36, wherein the protective layer is made of a material selected from the group consisting of: silicon dioxide, silicon nitride, and silicon oxynitride.